What is claimed is:

1. An apparatus, comprising:

a semiconductor device formed on a conductivity region; and

a low resistive path barrier formed surrounding the conductivity region to isolate the conductivity region from a substrate that supports the conductivity region and the low resistive path barrier.

2. The apparatus of claim 1, further comprises of a deep trench isolation formed surrounding the low resistive path barrier on the opposite side of the conductivity region.

3. The apparatus of claim 2, wherein the deep trench isolation extends into the substrate.

4. The apparatus of claim 1, wherein the conductivity region is at least one of n-type and p-type conductivity regions.

5. The apparatus of claim 1, wherein the semiconductor device is a selected one of CMOS, BiCMOS, NMOS and PMOS.

6. The apparatus of claim 1, wherein the low resistive path barrier is coupled to a power supply.

7. The apparatus of claim 1, wherein the substrate is selected from one of p-type and n-type substrate.

8. The apparatus of claim 1, wherein the low resistive path barrier comprises of a plug coupled to a buried layer.

9. The apparatus of claim 8, wherein the plug is coupled to a power supply.

10. The apparatus of claim 1, wherein the low resistive path barrier comprises a selected one of N+ and P+ doped material.

11. The apparatus of claim 1, wherein the deep trench isolation comprises of a selected one of a dielectric and an insulation material.

12. The apparatus of claim 1, wherein the substrate is biased to 0 volts.

13. The apparatus of claim 1, wherein the low resistive path barrier comprises of a first capacitive decoupling junction located at an interface between the low resistive path barrier and the conductivity region, and a second capacitive decoupling junction located at an interface between the low resistive path barrier and the substrate.

14. The apparatus of claim 7, wherein the plug having a resistivity of about 0.01 ohm-cm and the buried layer having a resistivity of about 0.005 ohm-cm.

15. The apparatus of claim 2, wherein the deep trench isolation having a depth of about 5 μm.

16. A method comprising:

forming a semiconductor device on a conductivity region; and

forming a low resistive path barrier that surrounds the conductivity region to isolated the conductivity region from a substrate that supports the conductivity region and the low resistive path barrier,

17. The method of claim 16, further comprises forming a deep trench isolation surrounding the low resistive path barrier on the opposite side of the conductivity region.

18. The method of claim 16, further comprises coupling the low resistive path barrier to a power supply.

19. The method of claim 16, wherein the semiconductor device is a selected one of CMOS, BiCMOS, NMOS and PMOS.

20. The method of claim 16, wherein the conductivity region is at least one of n-type and p-type conductivity regions.

21. The method of claim 16, wherein the formed low resistive path barrier comprises a plug coupled to a buried layer.

22. The method of claim 21, further comprises coupling the plug to a power supply.

23. The method of claim 17, wherein forming of deep trench isolation further comprises filling the deep trench isolation with a selected one of a dielectric or a insulation material.

24. The method of claim 16, wherein the formed low resistive path barrier comprises a selected one of N+ and P+ doped material.

25. A system, comprising:

an integrated circuit having a semiconductor device formed on a conductivity region, including

a low resistive path barrier formed surrounding the conductivity region to isolated the conductivity region from a substrate that supports the conductivity region and the low resistive path barrier;

a bus coupled to the integrated circuit; and

a networking interface coupled to the bus.

26. The system of claim 25, further comprises a deep trench isolation formed surrounding the low resistive path barrier on the opposite side of the conductivity region;

27. The system according to claim 25, wherein the low resistive path barrier is coupled to a power supply.

28. The system according to claim 25, wherein the semiconductor device is selected from one of CMOS, BiCMOS, NMOS and PMOS.

29. The system according to claim 25, wherein the low resistive path barrier comprises a selected one of N+ and P+ doped material.

30. The system according to claim 25, wherein the low resistive path barrier comprises of a plug and a buried layer.